2FHC0435

Application Manual

Compact gate driver core, supports multi-level

The 2FHC0435 is a dual-channel gate driver with electrical interface. It is also with ASIC digital control for safe and reliable driving of IGBT. The gate driver is suitable for all common IGBT up to 1800A/1700V and supports multi-level topologies.

The 2FHC0215 is a compact driver core with dimensions of 57mm*52mm and a maximum height of 18.6mm.

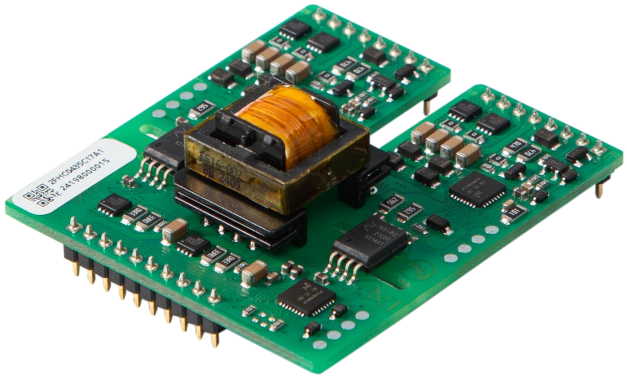

Fig.1 2FHC0435

Contents

Abstract

The 2FHC0435 is a compact IGBT driver core with complete dual-channel, which is developed by Firstack based on digital control, and has the isolated power supply, supply voltage monitoring, short-circuit protection and soft shut down, advanced active clamping, and intelligent fault management function.

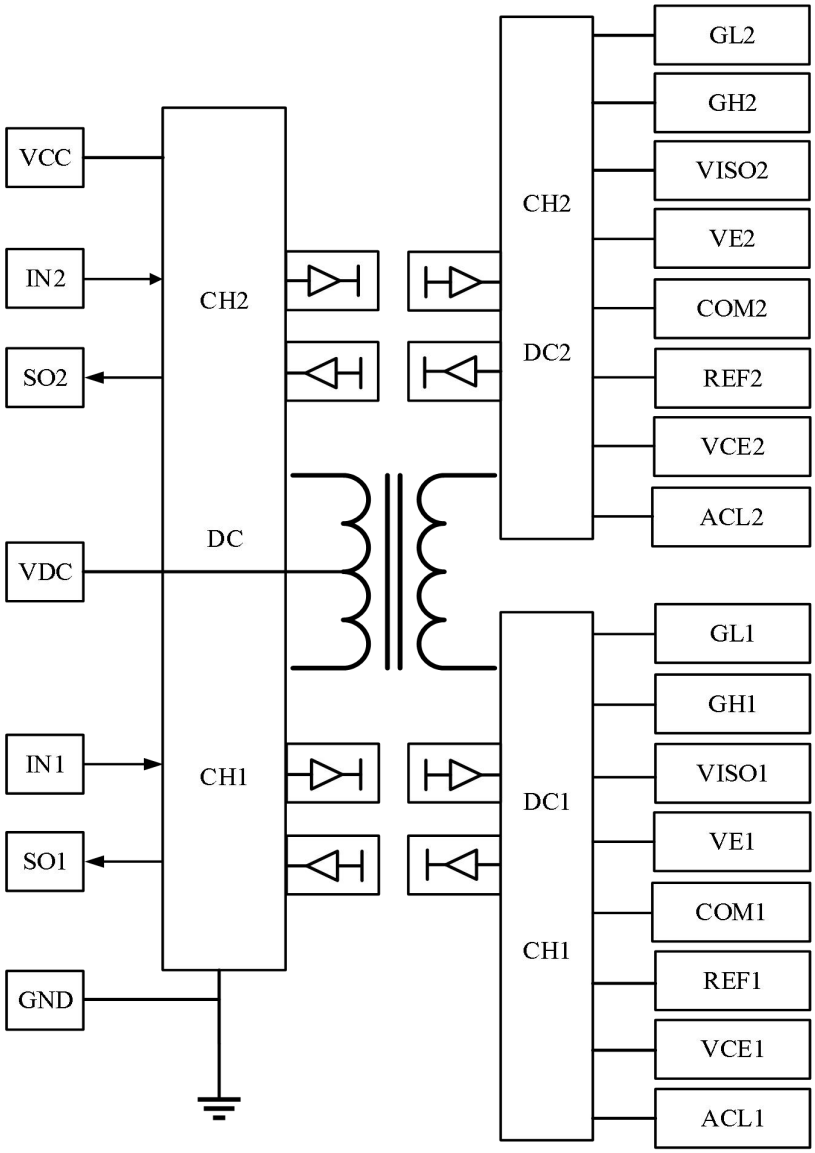

Fig.2 2FHC0435 functional block diagram

Pin Definition

Terminal	Pin	Definition	Function
P1	1	VDC	Supply voltage
	2	SO1	Status output channel 1, normal is high-impedance, fault is low
	3	SO2	Status output channel 2, normal is high-impedance, fault is low
	4	NC	Free
	5	NC	Free
	6	VCC	Primary side supply voltage
	7	GND	Ground
	8	IN1	Signal input channel 1
	9	IN2	Signal input channel 2
	10	GND	Ground
P2	11	ACL1	Active clamping feedback channel 1
	12	VCE1	V_{CE} sense channel 1: connect to IGBT collector of the module through diodes or resistor network
	13	REF1	Set V_{CE} detection threshold channel 1: resistor (Rthx) to VE1
	14	COM1	Negative power supply channel 1
	15	VE1	Emitter channel 1: (auxiliary) emitter connect to the power device
	16	VISO1	Positive power supply channel 1
	17	GH1	Gate high channel 1
	18	GL1	Gate low channel 1
P3	22	ACL2	Active clamping feedback channel 2
	23	VCE2	V_{CE} sense channel 2: connect to IGBT collector of the module through diodes or resistor network
	24	REF2	Set V_{CE} detection threshold channel 2: resistor (Rthx) to VE1
	25	COM2	Negative power supply channel 2

26	VE2	Emitter channel 1: (auxiliary) emitter connect to the power device
27	VISO2	Positive power supply channel 2
28	GH2	Gate high channel 2
29	GL2	Gate low channel 2

Primary Side Interface Description

1. Recommended Interface Circuit for Primary Side

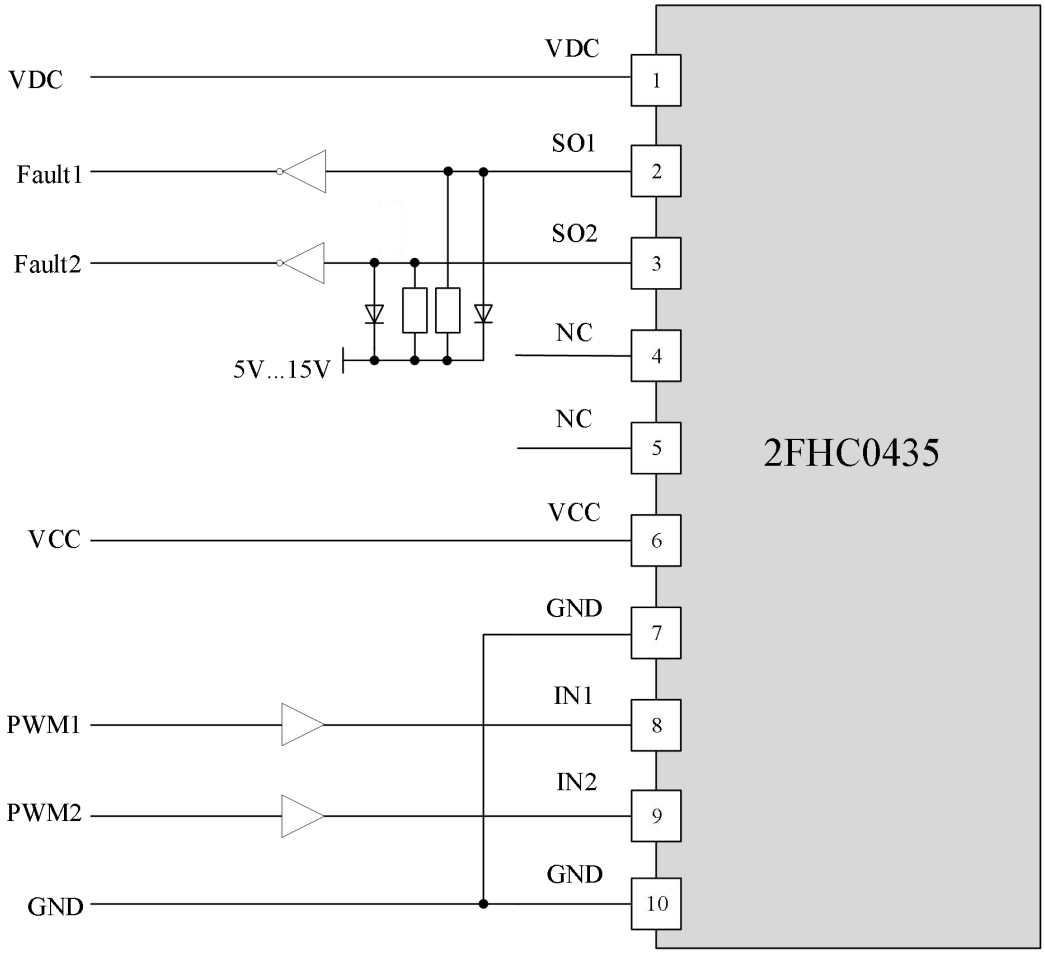

Fig.3 Peripheral interface recommended circuit for primary side

2. Primary Side Interface Description

The gate driver core 2FHC0435 is equipped with a 10-pin interface terminal on the primary side:

- 2x Power supply input terminal
- 2x Driving signal input terminal
- 2x Fault signal output terminal
- 2x GND(ground)
- 2x NC(free)

3. VDC&VCC

The 2FHC0435 is equipped with 2 power terminals, where VDC is used to supply power to the isolated DC/DC converter, VCC is used to supply power to the primary control circuits. The two power supplies can supply individually or separately, and it is recommended to share a 15V power supply.

The maximum power supply specification required for a single gate driver is 15V@1.1A. Customers can calculate the minimum power supply power required for the gate driver according to the following formula: gate driver power with load per channel* 2/80% + 2W.

4. INx

The signal input pin of the gate driver, supports 5-15V logic voltage, the resistance matching is important during design process, 33K-68K pull-down resistors are recommended.

The function of INx is related to the gate driver mode, which is set by software, and cannot be adjusted by external hardware.

Direct Mode：

IN1 and IN2 are independent. CH1 and CH2 can be turned on simultaneously.

Half bridge topology: To avoid a short-circuit caused by CH1 and CH2 being high at the same time, the control circuit must be set with sufficient dead time.

Half bridge Mode：

IN1 is the input terminal of drive signal (PWM), IN2 is the enable terminal of signal (EN);

If IN2 is low level, two outputs are blocked, all output signals are low level.

If IN2 is high level, two outputs are enabled, output signals are changing with IN1.

When IN2 is high level, IN1 turns from low to high, the gate signal of CH2 is blocked immediately, CH1 gate is turned on after dead time T_d.

Attention: The default dead time T_d is 4μs, which is set by software and can not be changed by hardware. When IN2 turns from low to high level, it needs to go through one dead time before the output changes with IN1.

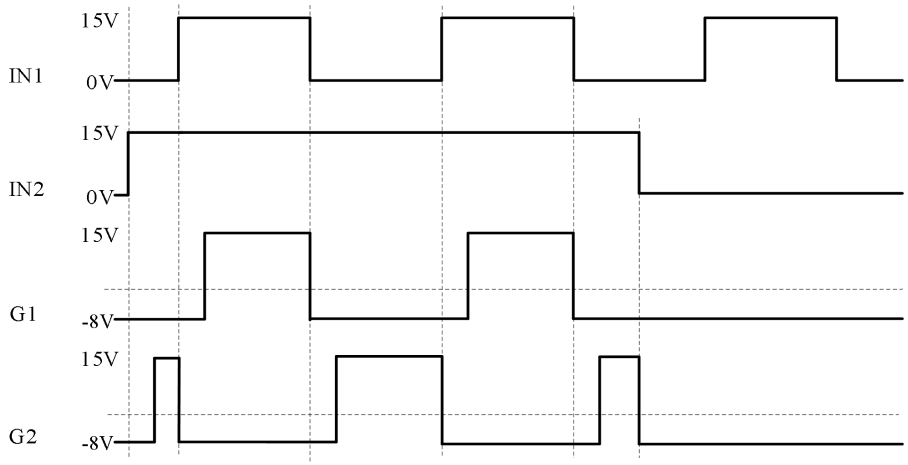

Fig.4 Logic diagram of half-bridge mode

5. SOx

The outputs SOx have open-drain transistors, which is by default a single fault signal to point the problem precisely. They can also be connected together to provide common fault signal.

Under fault condition, the current flowing through SOx can not exceeds 10mA defined in the data sheet.

When there is no fault, the output is high, the pull-up resistor is required to install in main control board. The recommended range of pull-up voltage is 5-15V, resistor value: 5V---3.3K-4.7K, 15V---10K-15K

When channel “x” detects fault, SOx will be low (connect to GND).

SOx Output Logic

When an undervoltage occurs on primary side of the driver, gate will be turned off directly with negative voltage and keep blocking for a blocking time, at the same time both of SOx goes to high after reporting 40ms low level fault.

If the undervoltage disappears before this process, SOx will keep high. If the undervoltage still exists, the fault will be pulled down again until it disappears, then return to high after a blocking time (80ms)

Primary side blocking signal: After the primary side undervoltage disappears, then after 80ms the blocking is over, primary side processes the INx signal normally.

When undervoltage occurs on secondary side of the gate driver, gate performs soft shut down first. When the negative voltage continues for a while, keep 0V turn-off and maintain blocking signal, the corresponding SOx signal reports 20ms low level fault and after that returns to high level for 100ms.

If the undervoltage disappears before the above process, SOx keep high; if the fault still exists, the fault signal will be pulled down again until the fault disappears, then after 80ms the SOx signal returns to high level.

Primary side blocking signal: After the secondary side undervoltage disappears, then after 60-80ms the blocking is over, primary side processes the INx signal normally.

Short-circuit fault:

When a short-circuit occurs on the secondary side of the gate driver, the gate first performs the soft shut down, then puts in a negative voltage to keep the shutdown state and maintains blocking signal, the corresponding SOx reports the fault, and then automatically restores the high level after pulling down for 10ms.

The 2FHC0435 is equipped with intelligent fault management function, please refer to "Intelligent Fault Management" in the manual for T_{SOX} details.

6. NC

The NC pin is not electrically connected to the inside of the gate driver, and if there is an external circuit connection to the NC pin, it will not affect the function of the gate driver.

Secondary Side Interface Description

1. Recommended Interface Circuit for Secondary Side

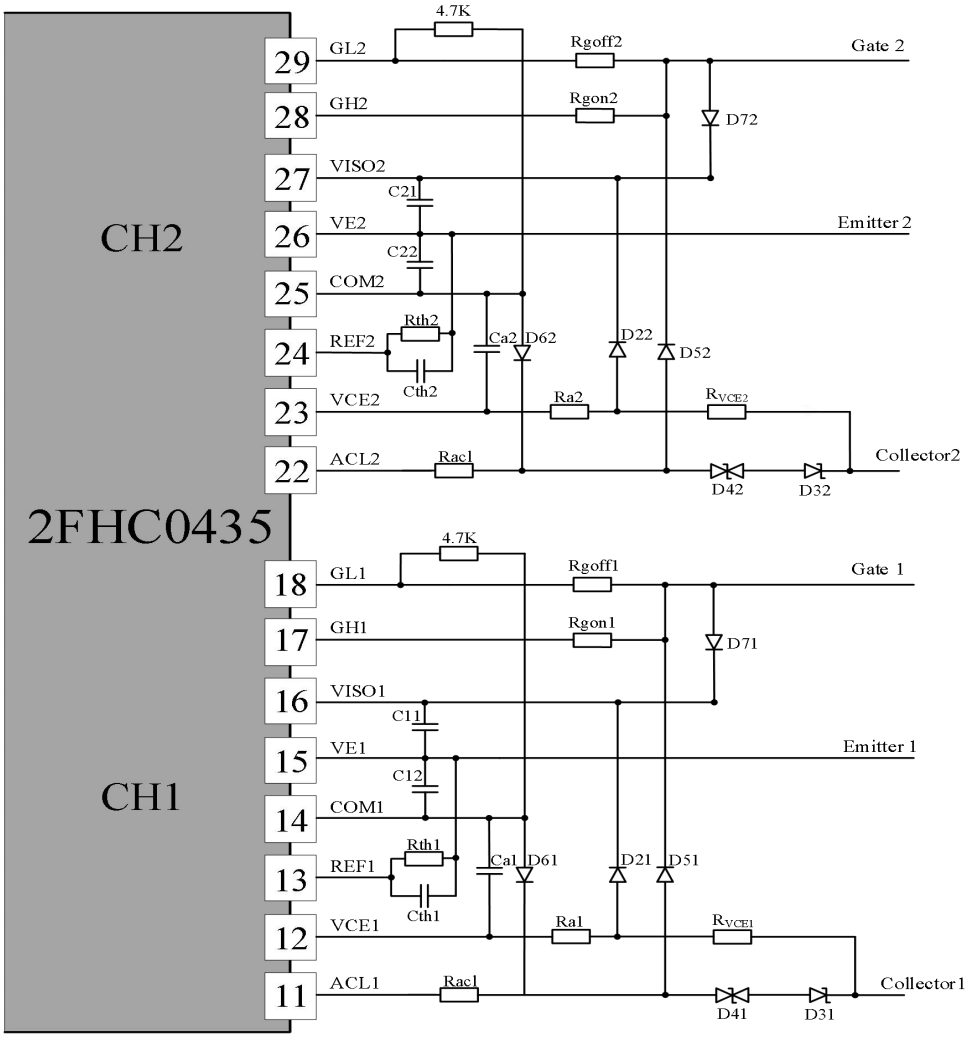

Fig. 5 Recommended circuit-resistor detection for secondary side

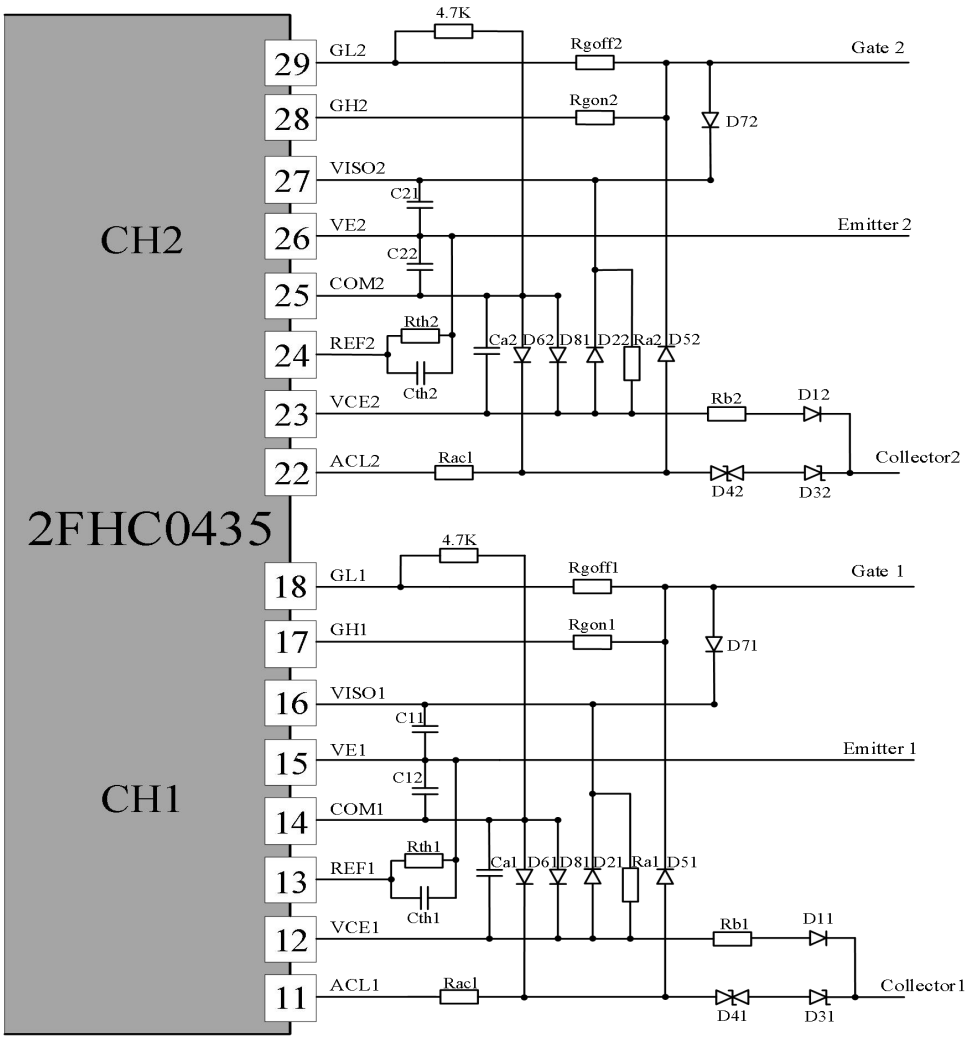

Fig.6 Recommended circuit-diode detection for secondary side

2. Secondary Side Interface Description

The secondary side of the gate driver has 2 channels CH1, CH2, each equipped with an 8-pin interface connector respectively:

- 1 x gate turn-off GLx
- 1 x gate turn-on GHx
- 1 x DC/DC positive output VISOx
- 1 x emitter VEx
- 1 x DC/DC negative output COMx
- 1 x reference REFx(short-circuit protection threshold)

- 1 x collector potential detection VCEx
- 1 x active clamping ACLx

3. Gate Driver Terminal (GHx & GLx)

The driver connects resistors to the gates of the IGBTs through the gate drive terminals. The GHx and GLx pins control the turn-on and turn-off of the IGBTs respectively, and the turn-on and turn-off resistors can be set separately as required. The design can be made with reference to '**Fig. 5/6**'.

It is recommended to connect a resistor over 4.7kΩ between GLx and COMx(or VEx). This resistor can provide a low impedance loop between the IGBT gate and emitter in case of the gate driver power down, and avoid floating voltage which causes the IGBT false turn-on.

Note that in multiple parallel applications, the resistance value after parallel connection shall not be less than 4.7kΩ.

Under IGBT short-circuit conditions, a too high VGE voltage will result in excessive short-circuit current, a clamp diode D7x can be added to the gate to clamp the gate voltage to VISOx, or a transient voltage suppressor D7 (D8) is connected between the gate and the emitter. Schottky diodes must not be used as gate clamp diodes, and transient voltage suppressor require consideration of breakdown voltage.

Please note that in half-bridge circuits, it is recommended not to generate waveforms for switching action on the IGBTs with a low supply voltage to the gate driver, otherwise too high rate of change of V_{CE} may lead to partial conduction of the IGBTs.

4. DC Power Supply and Emitter Terminal (VISOx, VEx, COMx)

The gate driver is designed for scalability by bringing out the positive power supply terminal VISOx, the negative power supply terminal COMx, and the emitter terminal VEx. DC-link capacitors can be matched on the secondary side of the DC/DC power supply.

IGBTs with a gate charge of 3uC or less can be driven without additional capacitor on the secondary side. For IGBTs with higher gate charge, it is recommended to place a certain amount of DC-link capacitors between VISOx-VEx and VEx-COMx in order to ensure that the logic level is stable when

the gate driver is in the switching state. According to the specification of the corresponding IGBT, when the Qg value is larger than 3uC, for every increase of 1uC, a minimum of 3uF capacitance is added to each of C11/C12/C21/C22. The capacitors should be placed as close as possible to VISOx, VEx, and COMx to reduce the amount of parasitic inductance. If the C1x and C2x capacitors exceed 150uF capacitance, please contact Firstack technical support.

It is recommended to use ceramic capacitors with withstanding voltage > 20V.

5. Detection Threshold (REFx)

This pin of the gate driver is internally connected to a 33k resistor pull-up to VISOx, and a Rthx is connected between REFx and VEx for setting the short-circuit detection voltage threshold. VREFx voltage calculation formula is:

$$\mathrm{VREFx} = \mathrm{VISOx} * \frac{\mathrm{Rthx}}{33\mathrm{k} + \mathrm{Rthx}}$$

It is recommended to connect a 68k resistor between REFx and VEx, at which point the VREFx value is 10.1V. This part of the circuit should be located as close as possible to the gate driver pins to reduce the amount of parasitic inductance, and it is recommended to increase the Cthx capacitance by 10-47pF to increase the immunity to interference of VREFx.

6. Collector Potential Detection Terminal (VCEx)

The 2FHC0435 collector potential detection supports both resistor detection and diode detection. It needs to be connected to the collector of the IGBT according to the corresponding recommended circuit to detect the short-circuit of the IGBT.

1) Resistor Detection

For the resistor detection circuit, refer to **Fig. 5**, "**Recommended circuit-resistor detection for secondary side**" in this manual.

It is recommended to set the resistance value R_{VCEX} so that the current I_{RVCEX}=0.6~1mA (e.g., for 1200V bus voltage, it is recommended to set the resistance value at (1.2~2MΩ), and the maximum resistance value is not more than 1mA.) It is possible to use a high voltage resistor or multiple resistors in series, and the design needs to take the voltage withstand ability and power consumption

of the resistor into consideration. The minimum creepage distance must be taken into account when designing PCB circuits.

The I_{RVCEX} can be calculated by the following:

$$I_{RVCEX} = \frac{VCx - V_{F(D2x)} - VISOx}{R_{VCEX}}$$

The diode D2x leakage current must be extremely low, the blocking voltage needs to be more than 40V, and Schottky diode cannot be used. Components Cax, Rax, and D2x should be located as close to the gate driver as possible to avoid excessive collector-emitter loops.

For detailed information on this part of the functional circuits, please refer to "**V_{CE} detection and short-circuit protection**" in this manual.

2) Diode Detection

The diode detection circuit can adapt to the low V_{CE} voltage, for the 2FHC0435, Firstack recommends to use the diode detection circuit.

For the resistor detection circuit, refer to **Fig.6**, "**Recommended circuit-diode detection for secondary side** ".

Recommended circuit component parameters are as follows:

- D1x: one US1M, for 650V IGBT
  two US1M, for 1200V IGBT
  two~three US1M, for 1700V IGBT
- Rax: 5kΩ~10kΩ, it is recommended that two or more 1206 resistors of equal power connected in parallel.
- Rbx: 100Ω~330Ω
- Cax: 100pF~1000pF
- D2x/D8x: Fast diodes, such as the BAS316, require low leakage currents over the full temperature range, blocking voltages higher than 40V, and Schottky diodes cannot be used.

When the Cax is small, the parasitic capacitance of the gate driver and PCB should be considered.

For details of the functional circuit, please refer to "**V_{CE} Detection and Short-circuit Protection**" in this manual.

3) Analog V_{CE} Sense and Shielding

Analog V_{CE} sense and shielding needs to be operated in the case of the gate driver without IGBT module, for testing and evaluating the gate driver function under weak power.

For the resistance detection circuit, if the module is not connected, the gate driver is provided with a turn-on signal, the driver gate will automatically respond; analog short-circuit sense can be realized by short-circuiting the D2x diode, it should be noted that the short-circuit response time is slightly larger than the actual value of the circuit design (the actual value needs to be measured in the strong power test platform, the CE terminal of the bus voltage applied).

For the diode detection circuit, if the module is not connected, the gate driver is provided with a turn-on signal, the gate driver will automatically detect a short-circuit fault, if the short-circuit response time is unstable, you can apply a voltage of 15V between the collector and emitter. Shielding of short-circuit detection needs to form a low impedance between the collector and the emitter, simulate the IGBT turn-on state, which can also be short-circuited, but at this time power supply to the CE terminal is not allowed.

7. Active Clamping (ACLx)

Active clamping partially turns the IGBT on when the voltage between the collector and emitter exceeds a preset threshold, thereby suppressing the collector-emitter voltage of the IGBT, which is operating in the linear region.

For the active clamping circuit, refer to the "**Recommended circuit for secondary side**" in this manual.

If the active clamping function is not required, the D3x, D4x, D5x, D6x diodes and Racl resistors can be omitted. The basic active clamping technology is a single-path feedback from the collector to the gate via a transient voltage suppressor (TVS). If only the basic active clamping is used, only the D3x, D4x, and D5x diodes need to be soldered, and the D6x diode and Racl resistor can be omitted.

The 2FHC0435 also supports the advanced active clamping function. When the advanced active clamping is required, in addition to feeding back the collector voltage to the gate through D3x, D4x, D5x, it is also necessary to solder the D6x diode and Racl to connect the feedback circuit to the gate driver ACLx pin. When the voltage to the left of the Racl resistor exceeds 10V, the gate driver will turn off the internal shutdown MOSFET and turn on the soft shut down MOSFET to improve the active clamping efficiency; and the active clamping performance can be improved by increasing the resistance value of the gate resistor Rgoffx.

TVS diodes D3x, D4x are connected in series to form an active clamping network, the figure is only schematic, the number of series and specifications need to choose according to the actual working conditions, in the case of the same total threshold, the active clamping efficiency can be improved by increasing the number of TVS. However, it should be noted that at least one of the TVS must be a bidirectional TVS (e.g., D4x in **Fig. 5/6**), which can avoid the negative current flowing through the TVS when the IGBT antiparallel diode is in forward recovery in the turn-on state, which will lead to undervoltage of the secondary power supply. The breakdown voltage and current will be different between different brands of TVS, it is recommended to debug and match according to the actual application.

Circuit devices specification are recommended as follow:

VDC-LINK=800V, 5 TVS of SMBJ130A and 1 TVS of SMBJ130CA are recommended.

VDC-LINK = 1200V, 5 P6SMB220A and 1 P6SMB220CA TVS are recommended.

D5x, D6x and D7x diodes are recommended to use fast recovery diodes with the withstand voltage larger than 40V. Depending on the application, the current larger than 1 A is recommended.

Please note that when setting the TVS threshold, it is necessary to avoid frequent TVS triggering during normal operation. The efficiency of the active clamping is highly dependent on the TVS type (manufacturer). When replacing the TVS, it is recommended to re-evaluate the test to avoid application risk.

Technical Principle

1. Power Supply and Electrical Isolation

This gate driver implements isolated power and signal. Power isolation is realized by the transformer, signal isolation is realized by capacitive coupling. The transformer complies with the safety isolation standard EN50178 and the primary and secondary sides fulfil protection class 2.

Please note that a stable supply voltage and current are required to power the driver.

2. Power Monitoring

The primary side, as well as the two secondary side power supplies of the gate driver have local power detection circuits, and corresponding undervoltage protection.

When undervoltage occurs in the primary side power supply, both IGBTs are driven by the negative gate voltage to maintain the turn-off state (both channels are blocked), and both SO1 and SO2 feed back the fault status signal to the master computer.

When the positive or negative voltage on the secondary side is lower than the threshold voltage, the driver circuit will determine that an undervoltage fault has occurred, the driver circuit will automatically block the IGBT, and at the same time, the corresponding SOx will feedback a fault signal to the master computer.

The SOx outputs are automatically reset after the primary and secondary side undervoltage faults are removed.

Firstack recommends against operating either IGBT in the bridge arm in an undervoltage state.

Due to the presence of C_{CG}, when one IGBT in the bridge arm turns on, the high dv/dt from it can be coupled to the other IGBT through the C_{CG}, resulting in micro-conductance of the other IGBT.

3. V_{CE} Sense and Short-circuit Protection

1) Resistor Detection

Resistor detection recommended circuit please refer to **Fig.5**, "**Recommended circuit-resistor detection for secondary side**" of this manual.

In the IGBT off state, the internal MOSFET of the gate driver will connect VCEx to VCOMx, at this time, the VCax voltage is equal to the negative supply voltage, and when the bus voltage is low, the current flows to VCOMx through the R_{VCEx} and Rax resistor network; when the bus voltage is high, the voltage on the right side of the Rax resistor is clamped by the D2x diode to VISOx, at this time, the excess current will flows to VISOx through the R_{VCEx} resistor network and the D2x diode.

The Rthx resistor in the diagram is used to set the short-circuit detection reference threshold, refer to **Detection Threshold (REFx)** for information.

The driver's external Rax resistor and Cax capacitor are used to set the response time and enhance the versatility of the gate driver.

The response time is the time from the moment the IGBT is turned on until the gate driver detects a short-circuit fault and begins to act on the soft shutdown protection, which is close to the short-circuit duration. The detection circuit of each channel of the 2FHC0435 is independent. When a short-circuit fault is detected, the gate driver turns off the corresponding IGBT, and the fault state is immediately transmitted to the corresponding SOx outputs after a blocking time Tb, the gate driver resumes processing the input signal.

The response time of the 2FHC0435 consists of three parts: SCS time (software blanking time, about 3us), Cax charging time, and SC filtering time (Tsc_filter time, referred to as Tsc_ft, which is set as about 1us by the gate driver).

The SCS time refers to the time from IGBT turn-on until the gate driver's internal chip starts to short-circuit detection, the Cax charging time is the time from gate turn-on to the time the V_{CE}x voltage reaches the V_{CE} monitoring threshold, and the SC filtering time is the time from the V_{CE}x voltage exceeds the V_{CE} monitoring threshold to the time the gate driver determines that a short-circuit fault has occurred.

The relationship between the three is as follows: when SCS time > Cax charging time, the response time is equal to SCS time + SC filter time; when SCS time < Cax charging time, the response time is equal to Cax charging time + SC filter time. Where SCS time and SC filter time are programmed, SCS time + SC filter time ≈ 4μs.

The response time Tax required for turn-on can be set according to the following formula:

$$Tax = Tsc\_ft + Rax * Cax * \ln(\frac{VISOx + V_{F(D2x)} + |VCOMx|}{VISOx + V_{F(D2x)} - VREFx})$$

Description:

When the set response time Tax≤4μs, Tax=4μs;

When the set response time Tax＞4μs, Tax is the set value.

The following table lists the response time Tax corresponding to different Cax values and Rthx values (RVCEX=1.8MΩ, Rax=120kΩ) for setting the desired response time.

Cax(pF)	Rthx(kΩ)/VREFx(V)	Tax(μs)
0	68/10.1	4
15	68/10.1	5.9
22	68/10.1	7
33	68/10.1	8.9
47	68/10.1	11.8
0	24.9/6.4	4
15	24.9/6.4	4.3
22	24.9/6.4	5.1
33	24.9/6.4	6.3
47	24.9/6.4	8.4

Table 1 Resistor detection response time Tax vs. Cax capacitor and Rthx resistor table

Since the presence of parasitic capacitance in practice may affect the response time, it is recommended that actual measurement be made in the final design. When defining the response time, it is important to ensure that it is less than the maximum short-circuit duration allowed for the power semiconductor used.

The resistance detection response time has a minimum bus voltage requirement for the bus voltage. The response time increases when the DC bus VDC is <550V or when the threshold voltage VREFx is high, and decreases when VREFx is low.

2) Diode Detection

The diode detection circuit can accommodate low V_{CE} voltage, and for the 2FHC0435, Firstack recommends the diode detection circuit. For the recommended circuit, please refer to **Fig. 6**, "**Recommended circuit-diode detection for secondary side**" of this manual.

Consistent with resistor detection, in the IGBT off state, the gate driver's internal MOSFET will connect V_{CE}x to V_{COM}x, at which time the V_{Cax} voltage is equal to the negative supply voltage. When the IGBT is on, V_{ISOx} charges the Cax capacitor through the Rax resistor. If the IGBT is saturated and on, the collector potential is reduced to the V_{CEsat} value, and the V_{Ca}x voltage will be affected by the D1x clamp and be at a low level.

The formula for calculating the voltage across Cax is as follows:

$$\mathrm{VCax} = \mathrm{VCEsat} + \mathrm{VF(D1x)} + \mathrm{Rbx} * \frac{\mathrm{VISOx} - \mathrm{V_{F(D1x)}} - \mathrm{V_{CEsat}}}{\mathrm{Rax} + \mathrm{Rbx}}$$

The value of the SC detection threshold voltage V_{REF}x must be higher than Vcax for normal saturation turn-on, and the recommended V_{REF}x value for the 2FHC0435 is 10.1V.

Rax and Cax can be used to set the response time Tax required for turn-on according to the following equation:

$$\mathrm{Rax[k\Omega]} = \frac{\mathrm{T_{ax}[us]} - \mathrm{Tsc\_ft}}{\mathrm{Cax[pF]} * \ln\left(\frac{\mathrm{VISOx} + |\mathrm{VCOMx}|}{\mathrm{VISOx} - \mathrm{VREFx}}\right)}$$

When Cax is selected at a small value, the parasitic capacitance of the gate driver and PCB need to be considered.

The following table lists the response time Tax (Rax=10kΩ) corresponding to different Cax values for setting the desired response time.

Cax(pF)	Rthx(kΩ)/VREFx(V)	Tax(μs)
100	68/10.1	4
220	68/10.1	4.6

330	68/10.1	6.4
470	68/10.1	8.5
680	68/10.1	11.8

Table 2 Resistor detection response time Tax vs. Cax capacitor and Rthx resistor table

Description: When the set response time Tax≤4μs, Tax=4μs;

When the set response time Tax＞4μs, Tax is the set value.

4. Soft Shut Down (SSD)

The 2FHC0215 series gate drivers are configured with SSD function.

When IGBT desaturation occurs, V_{CE} reaches the bus voltage. At the same time, the I_C will reach 4 times of the rated current or even more and the di/dt at the turn-off time will form a very high voltage peak on the parasitic inductance, which will easily damage the IGBT.

When IGBT desaturation is triggered, the digital core will detect and trigger soft shut down to turn off the IGBT, the IGBT is gradually turned down by slowly lowering the gate voltage Vge, which effectively reduces the di/dt, and then reduces the voltage peak at the shutdown moment. Thus, the short-circuit protection of IGBT is achieved. In normal operation (e.g. at rated current or overcurrent) it is not enabled. Therefore, it is necessary to adapt a suitable shutdown resistor according to the actual operating conditions, or to take appropriate measures to avoid excessive shutdown peaks during normal operation.

The SSD function also has its limitations on the suppression of turn-off peaks, excessive DC bus stray inductance can still lead to large turn-off peaks under short-circuit conditions. Therefore, it is necessary to analyse the short-circuit behaviour of IGBTs in all kinds of extreme operating conditions. Firstack suggests that it is best to simulate the actual operating conditions for short-circuit testing to ensure that the V_{CE} of IGBTs in short-circuit conditions has sufficient safety margins.

If the V_{CE} voltage peak is too high and cannot be reduced by other means, Firstack recommends using the basic active clamping function.

5. Intelligent Fault Management

The gate driver detects the operation status of the module in real time, and when the module fails, it uploads the fault status to the master computer through the SOx output, and the 2FHC0435 realizes the fault differentiation by the difference of the pull-down time of the SOx signal (the fault return time).

For more information, see the table below.

Fault Type	**Short-circuit**	**Undervoltage(Sec.)**	**Undervoltage(Pri.)**	**Other Faults**
Return time (TSOx)	10ms	20ms	40ms	80ms

Technical Support

Firstack's professional team will provide you with business consultation, technical support, product selection, price, lead time and other related information, and guarantee to answer your questions within 48 hours.

Legal Disclaimer

This manual gives a detailed introduction about the product, but cannot promise to provide specific parameters. No warranty or guarantee, express or implied, is given herein as to the delivery, performance or applicability of the product.

Firstack reserves the right to modify technical data and product specifications at any time without prior notice. Firstack's general payment terms and conditions apply.

Company Information

Tel: +86-571 8817 2737

Fax: +86-571 8817 3973

Web: www.firstack.com

Email: fsales@firstack.com

Address: 4-5/F, Building/5, Xizi Wisdom Industrial Park, No.1279 Tongxie Road, Hangzhou, China